

**LISTING OF THE CLAIMS**

1. (Currently Amended) A liquid crystal display device, comprising:
  - a first substrate;
  - a main seal on the first substrate and defining a liquid crystal injection area;
  - a first step-shaped compensating layer under the main seal;
  - a plurality of dummy seals on the first substrate and external to the liquid crystal injection area; and
  - a second step-shaped compensating layer under the plurality of dummy seals, the second step-shaped compensating layer having substantially a same ~~thickness~~ structure as the first step-shaped compensating layer.
2. (Original) The liquid crystal display device according to claim 1, wherein the main seal is provided with a liquid crystal injection hole through which a liquid crystal can be injected.
3. (Original) The liquid crystal display device according to claim 1, wherein the main seal and the dummy seals have a same thickness.
4. (Previously Presented) The liquid crystal display device according to claim 1, wherein the first step-shaped compensating layer has a thickness of about 6500Å.
5. (Original) The liquid crystal display device according to claim 1, wherein a top of the main seal and tops of the dummy seals are a same distance from the first substrate.
6. (Original) The liquid crystal display device according to claim 1, further comprising:
  - a gate metal pattern on the substrate forming a gate line and a gate electrode; and
  - a gate-insulating layer covering the gate metal pattern.
7. (Previously Presented) The liquid crystal display device according to claim 6, wherein the first and second step-shaped compensating layers include the gate metal pattern and the gate-insulating layer.
8. (Original) The liquid crystal display device according to claim 6, wherein the main seal and the dummy seals are formed on the gate-insulating layer.

9. (Withdrawn) A method of fabricating a liquid crystal display device, comprising the steps of:

forming a first step coverage-compensating layer having a desired thickness on a substrate;

forming a main seal defining a liquid crystal injection area on the first step coverage-compensating layer;

forming a second step coverage-compensating layer having the same thickness as the first step coverage-compensating layer on the substrate; and

forming a plurality of dummy seals on the second step coverage-compensating layer in such a manner to be arranged at the outer side of the main seal.

10. (Withdrawn) The method according to claim 9, wherein one side of the main seal is provided with a liquid crystal injection hole through which a liquid crystal is injected.

11. (Withdrawn) The method according to claim 9, wherein the main seal has the same thickness as each of the dummy seals.

12. (Withdrawn) The method according to claim 9, wherein each of the first and second step coverage-compensating layers has a thickness of about 6500Å.

13. (Withdrawn) The method according to claim 9, further comprising the steps of:

forming a gate metal pattern formed on the substrate and then patterning the gate metal layer into a gate line supplied with a scanning signal and a gate electrode of a thin film transistor;

disposing a gate-insulating layer, an active layer, an ohmic contact layer and a source/drain metal layer in such a manner to cover the gate metal pattern;

patterning the ohmic contact layer and the source/drain metal layer in such a manner to be left on the thin film transistor and be removed at the formation positions of the main seal and the dummy seals;

forming the passivation layer on the gate-insulating layer in such a manner to cover the source/drain metal layer;

forming a photo resist into a uniform thickness on the passivation layer;

patterning the photo resist such that the photo resist on the thin film transistor is left to have a different thickness and the photo resist is removed from said positions of the main seal and the dummy seals;

patterning the passivation layer and a semiconductor layer by utilizing the photo resist pattern as a mask such that the passivation layer and the semiconductor layer is removed from said positions of the main seal and the dummy seals and such that the passivation layer on the thin film transistor is left and the drain electrode patterned into the source/drain metal layer is exposed; and

forming a pixel electrode electrically connected, via a contact hole for exposing the drain electrode, to the drain electrode to drive a liquid crystal, on the passivation layer.

14. (Withdrawn) The method according to claim 13, wherein each of the first and second step coverage-compensating layers includes the gate metal pattern and the gate-insulating layer.

15. (Withdrawn) The method according to claim 13, wherein the main seal and the dummy seals are formed on the gate-insulating layer.

16. (Withdrawn) A method of compensating for a cell gap between liquid crystal cells in a liquid crystal display device, comprising the steps of:

forming a first step coverage-compensating layer having a desired thickness on a substrate and forming a main seal defining a liquid crystal injection area thereon; and

forming a second step coverage-compensating layer having the same thickness as the first step coverage-compensating layer in such a manner to be arranged at the outer side of the main seal and disposing the dummy seals thereon so as to eliminate a step coverage between the main seal and the dummy seals, to thereby uniform a cell gap between the liquid crystal cells.

17. (Withdrawn) The method according to claim 16, wherein the first step coverage-compensating layer and the second step coverage-compensating layer are made from the same material and have the same stacked-layer number.

18. (Withdrawn) The method according to claim 16, wherein one side of the main seal is provided with a liquid crystal injection hole through which a liquid crystal is injected.

19. (Withdrawn) The method according to claim 16, wherein the main seal has the same thickness as each of the dummy seals.

20. (Withdrawn) The method according to claim 16, wherein each of the first and second step coverage-compensating layers has a thickness of about 6500Å.

21. (Currently Amended) A liquid crystal display device, comprising:  
a first substrate;  
a main seal on the first substrate and defining a liquid crystal injection area;  
a first compensating layer with a width substantially the same as a width of the main seal disposed between the first substrate and the main seal;  
a plurality of dummy seals on the first substrate and external to the liquid crystal injection area; and  
a second compensating layer with a width substantially the same as a width of the dummy seals disposed between the first substrate and the plurality of dummy seals, the second compensating layer having substantially a same ~~thickness~~ structure as the first compensating layer.

22. (Previously Presented) The liquid crystal display device according to claim 21, wherein the main seal is provided with a liquid crystal injection hole through which a liquid crystal can be injected.

23. (Previously Presented) The liquid crystal display device according to claim 21, wherein the main seal and the dummy seals have a same thickness.

24. (Previously Presented) The liquid crystal display device according to claim 21, wherein the first compensating layer has a thickness of about 6500Å.

25. (Previously Presented) The liquid crystal display device according to claim 21, wherein a top of the main seal and tops of the dummy seals are a same distance from the first substrate.

26. (Previously Presented) The liquid crystal display device according to claim 21, further comprising:

a gate metal pattern on the substrate forming a gate line and an gate electrode; and  
a gate-insulating layer covering the gate metal pattern.

27. (Previously Presented) The liquid crystal display device according to claim 26, wherein the first and second compensating layers include the gate metal pattern and the gate-insulating layer.

28. (Previously Presented) The liquid crystal display device according to claim 26, wherein the main seal and the dummy seals are formed on the gate-insulating layer.